REMARKS

Present Status of the Application

The Office Action rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by Horan et al. (U. S. Patent 5,892,964; hereinafter Horan). Applicant has amended claims 1, 10 and 13. After entry of the amendments, claims 1-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by Horan. Applicant respectively traverses the rejections for at least the reasons set forth below.

As for example shown in FIG 2, the claimed bridge 230 is between the AGP bus 220 and the extended bus 245. The AGP bus 220 is coupled to the control chip set 200. The control chip set 200 is then coupled to the CPU 10, the system memory 11, and the bus 240. IN other words, the bridge 230 is not directly coupled to the control chip set 200, which has the has the north bridge and the couth bridge as shown in FIG 1. The features have recited in amended claims.

In re Horan in Fig. 3A, the logic chip set 218c is coupled to the CPU interface 202 and the memory interface 204, and the PCI bus 109. Then, the AGP buses 302, 304 are ***directly*** coupled to the logic chip set 218c. There is no addition bridge, like the claimed bridge of the invention, being disclosed. In Fig. 4A, again, the core logic 104 is coupled with the CPU 102, the PCI bus 109, and the memory 106. The core logic 104 is like the control chip set in the

present invention. Then two AGP bus 416a, 416b are directly coupled to the core logic 104.

However, Horan failed to disclose the addition bridge 230 coupled between the original AGP bus and an extended bus. Independent claims 1, 10, and 13 should be patentable.

Further still, with respect to claims 2, 4, and 10, the bridge 230 has the structure as shown in FIG. 3. As discussed above, the logic chip set 218a (see Fig. 3) or 218c (see Fig. 3A) of Horan is not the addition bridge but is the control chip set, which directly coupled with the CPU, the system memory, and the main PCI bus.

Further still, with respect to claims 5, 12, and 14, with the second bridge 250 can be further included for extending the bus 265. Horan failed to disclose these features.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 10, and 13 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-12, and 14-15 patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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